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Design of Dual Dynamic Flip-Flop with Featuring Efficient Embedded Logic for Low Power Cmos Vlsi Circuits

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Abstract-In this paper, we introduce a new dual dynamic node hybrid flip-flop (DDFF) and a novel embedded logic module (DDFF-ELM) based on DDFF. The proposed designs eliminate the large capacitance present in the pre-charge node of several state-of-the-art designs by following a split dynamic node structure to separately drive the output pull-up and pull down transistors. The aim of the DDFF-ELM is to reduce pipeline overhead. It presents an area, power, and speed efficient method to incorporate complex logic functions into the flip-flop. The performance comparisons made in a 90 nm technology when compared to the Semi dynamic flip-flop, with no degradation in speed performance. The leakage power and process-voltage-temperature variations of various designs are studied in detail and are compared with the proposed designs.

Index Terms- Flip-flops, high-speed, leakage power, low-power.

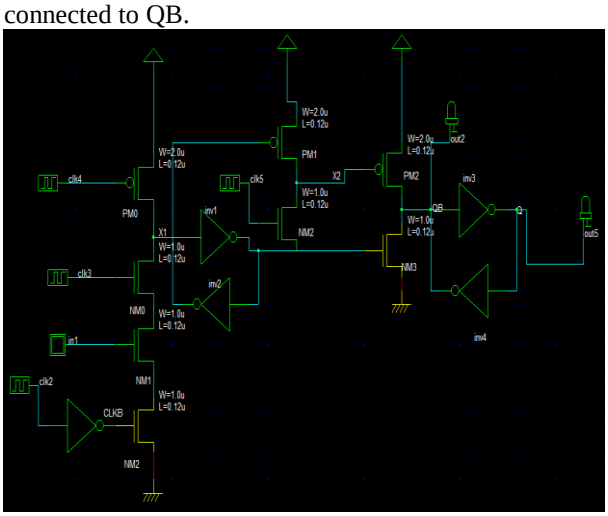
I. INTRODUCTION

Technology and speed are always moving forward, from low scale integration to large and VLSI and from megahertz (MHz) to gigahertz (GHz). The system requirements are also rising up with this continuous advancing process of technology and speed of operation. Very large Extensive work has been devoted to improve the performance of the flip-flops in the past few decades. Hybrid latch flip-flop (HLFF) and semi dynamic flipflop (SDFF) are considered as the classic high-performance flip-flops.

Flip-flop architecture named cross charge control flip flop (XCFF), which has considerable advantages over SDFF and HLFF in both power, area and speed. It uses a split-dynamic node to reduce the pre charge capacitance, which is one of the most important reasons for the large power consumption in most of the conventional designs. Redundant power dissipation that results when the data does not switch for more than one clock (CLK) cycles. It has large hold-time requirement makes the design of timing-critical systems with XCFF. Finally, despite having a single data-driven transistor, embedding logic to XCFF is not very efficient due to the susceptibility to charge sharing at the internal dynamic nodes. In this paper, we propose a new dual dynamic node hybrid flip-flop (DDFF) and a novel embedded logic module (DDFFELM). Both of them eliminate the drawbacks of XCFF.

II. Previous Method

Dual Dynamic Hybrid Flip Flop(DDFF) which has extra inv4 occupies an additional area to flip flop and then its requires more power. QB in the output is inverted by inv3,gets output as Q. So the output Q is again inverted and its not required. One of the most drawback of DDFF is large area and more power.Inv4 which causes error when its connected to QB.



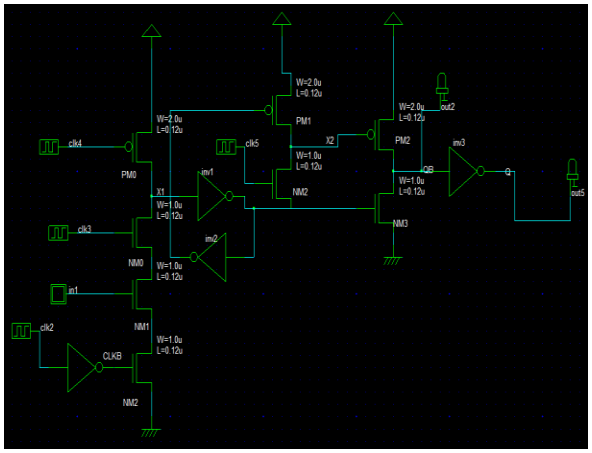
Schematic Diagram of DDFF

III. PROPOSEDDDFF ARCHITECTURE

In the proposed DDFF architecture,NodeX1 is pseudo-dynamic, with a weak inverter acting as a keeper, whereas, compared to the XCFF, in the new architecture node X2 is purely dynamic. An unconditional shutoff mechanism is provided at the frontend instead of the conditional one in XCFF. The operation of the flip-flop can be divided into two phases: 1) the evaluation phase, when CLK is high,

and 2) the pre charge phase, when CLK is low. The actual latching occurs during the 1–1 overlap of CLK and CLKB during the evaluation phase. If Dis high prior to this overlap period, node X1 is discharged through NM0-2. This switches the state of the cross coupled inverter pair INV1-2 causing node X1B to go high and output QB to discharge through NM4. The low level at the nodeX1 is retained by the inverter pair INV1-2 for the rest of the evaluation phase where no latching occurs. Thus, nodeX2 is held high throughout the evaluation period by the pMOS transistorPM1. As the CLK falls low, the circuit enters the pre charge phase and node X1 is pulled high through PM0, switching the state of INV1-2. During this period node X2 is not actively driven by any transistor, it stores the charge dynamically. The outputs at node QB and maintain their voltage levels through INV3-4. If Dis zero prior to the overlap period, node X1 remains high and nodeX2 is pulled low throughNM3astheCLK goes high. Thus, node QB is charged high through PM2 andNM4 is held off. At the end of the evaluation phase, as the CLK falls low, node X1 remains high andX2 stores the charge dynamically. The architecture exhibits negative setup time since the short transparency period defined by the 1–1 overlap CLK of and CLKB allows the data to be sampled even after the rising edge of the CLK before CLKB falls low.

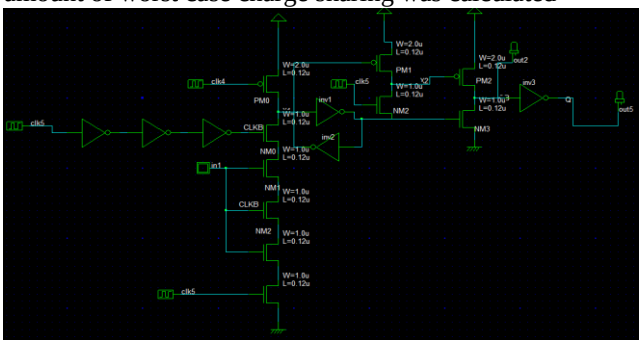
NodeX1 undergoes charge sharing when the CLK makes a low to high transition while Dis held low. This results in a momentary fall in voltage at nodeX1, but the inverter pair INV1-2 is skewed properly such that it has a switching threshold well below the worst case voltage drop at nodeX1 due to charge sharing. The timing diagram shows that node X2 retains the charge level during the pre charge phase when it is not driven by any transistor. Note that the temporary pull down at node X2 when sampling a "one" is due to the delay between X1 andX1B.



Schematic Diagram Of Proposed DDFF

IV. PROPOSEDELM

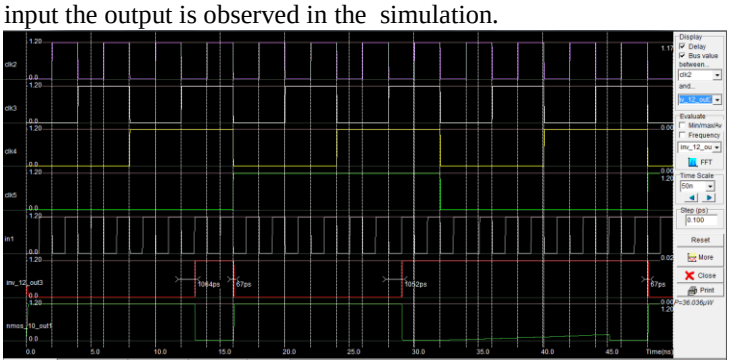
Dual dynamic node hybrid flip-flop with logic embedding capability (DDFF-ELM) transistor driven by the data input is replaced by the PDN and the clocking scheme in the frontend is changed. The reason for this in clocking is the charge sharing, which becomes uncontrollable as the number of nMOS transistors in the stack increases. The same reason makes XCFF also incapable of embedding complex logic functions. In order to get a clear picture of the charge sharing in XCFF, it was simulated with different embedded functions and the amount of worst case charge sharing was calculated



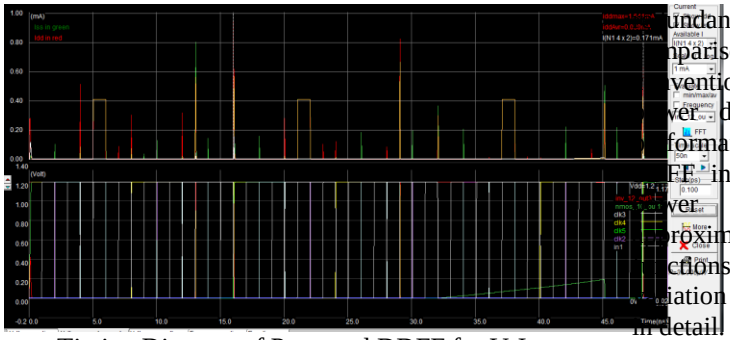
Schematic Diagram Of DDFF-ELM

V. RESULTS

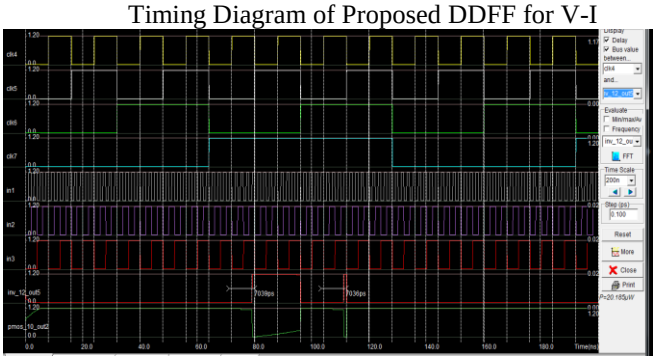
A simulation window appears with inputs and output. The power consumption is also shown on the right bottom portion of the window. If you are unable to meet the specifications of the circuit change the transistor sizes. Generate the layout again and run the simulations till you achieve your target delays. Depending on the input sequences assigned at the input the output is observed in the simulation.



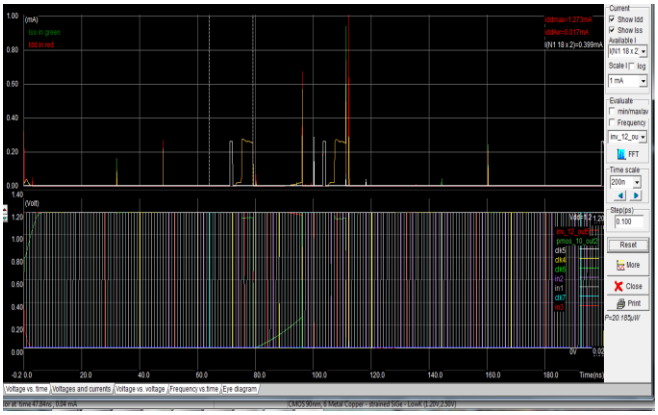
Timing Waveform of Proposed DDFF



Timing Diagram of Proposed DDFF for V-I



Timing Waveform of Proposed DDFF-ELM



Timing Diagram of Proposed DDFF-ELM for V-I

Flip Flop	No of transistors	Total power (µW)	Total Area (μm^2)	Total Current (mA)
DDFF	18	38.036	177	1.344
Proposed DDFF	16	5.371	171	1.300
DDELM	22	40.067	244	1,273

Performance Comparison of Various Flip-Flops

VI. CONCLUSION

In this paper, a new low power DDFF and a novel DDFFELM were proposed. An analysis of the overlap period required to select proper pulse width was provided in order to make the design process simpler. The proposed DDFF eliminates the undant power dissipation present in the XCFF. A mparison of the proposed flip-flop with the ventional flip-flops showed that it exhibits lower wer dissipation along with comparable speed formances. The presented ELM outperforms the FF in the CLK driving power and in internal wer dissipation. A power reduction of roximately 26% was observed when basic ctions were embedded. The leakage and PVT iation performances of the flip-flops were studied in detail.

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